Computer Architecture
Spring 2017

Homework No. 7
(Due on May 31)

1. Assume that 'slt $1, $2, $3' is executed with the implementation in Lecture note Chap 4, p. 25. Identify the value of the 9-bit control signals. (10)

2. Assume that 'jr $ra' is executed with the implementation in Lecture note Chap 4, p. 29. Identify the value of the 10-bit control signals. (10)

3. For the pipeline of the table of Lecture note p. 33 of Chap 4, what is the speed up compared to nonpipelined CPU for executing 100 instructions? (10) What is the maximum speed up of the pipelined CPU? (5)

4. Refer to the figure in Lecture note p. 42 of Chap 4. Assume that C = D + F (not B + F), and D is at memory [16($t0)]. Use $t6 to keep D. Give the code without delayed load (the code of left-hand side) and draw the timing diagram shown in the class. You need to put bubble and forwarding link in the diagram as necessary. How many cycles are taken? (10) Repeat the problem with the delayed load technique. (15)